SILICON-BASED MICROMACHINED PACKAGES FOR DISCRETE COMPONENTS

Rashaunda M. Henderson and Linda P. B. Katehi

The Radiation Laboratory
The University of Michigan, Ann Arbor, MI 48109-2122
USA

ABSTRACT

A novel approach has been taken to develop low cost, high frequency (Ka-band), electronic packages. An existing thick film package for a phase shifter chip has been redesigned using silicon as the base material. This paper reports on the fabrication techniques and the measurement improvement found by coupling silicon micromachining techniques with standard IC processing.

1.0 INTRODUCTION

For several years, electronic packaging for microwave components and systems has taken the back seat to high frequency circuit design and development. While state of the art high frequency components and devices have been realized, the package has been found to cause system degradation with increased frequency. The electronic package provides physical and thermal protection as well as interconnection to subassemblies. In recent years, packaging has received increasing attention and efforts are underway to produce low cost, high quality, high frequency structures.

As a result, MCMs, hybrid and monolithic packages have been developed using cofired ceramic, printed wiring board and thick and thin film technologies. In addition to package design there has been a serious effort in developing commercial modeling tools that can predict the performance of packages in the circuit environment [1]. At this time, high quality packages are being made which tend to be quite expensive and excessive in volume and weight, characteristics that prevent them from wide use [2].

In view of the above, the capability to create a low cost, low weight and volume package which operates at high frequency, demonstrates high bandwidth characteristics, and offers physical protection while not degrading performance, would provide major advances in packaging. At The University of Michigan we have been able to successfully incorporate IC processing techniques with silicon micromachining to fabricate silicon-based packages for discrete and monolithically integrated components. Given the knowledge base developed in silicon micromachining, the goal is to take advantage of the electrical and mechanical properties of single crystal silicon so as to create low cost, high precision, miniature microwave and millimeter wave packaged components.

2.0 BACKGROUND/DESIGN/FABRICATION

Recent work, [3], has led to the development of self-packaged components that have excellent isolation from neighboring elements in addition to individual component protection. Self-packaged silicon components are an alternative to conventional structures, appropriate for low cost, low volume, miniaturized high density subsystems.

Silicon is the best substrate to use when it comes to high frequency packaging components. The mechanical properties as presented by Petersen [4] are excellent and comparable to certain metals. Using micromachining and IC processing techniques, via hole diameter and linewidth dimensions are the smallest possible, which is very much desired for the reduction of high frequency parasitics. The thermal conductivity of Ga As, In P, and Ge (80,65,68), (W/(m*K)) creates problems with heat dissipation. As compared to 92% alumina (18), Si (135) is an excellent heat sink, which makes it a very good packaging material [5]. By combining the electrical and mechanical advantages of silicon, low cost batch fabricated packaged components can be incorporated on-wafer to increase circuit density while remaining low in volume.

A package fabricated by Hughes Aircraft for NASA Lewis served as the model for this design. The high temperature cofired ceramic (HTCC) process is used to develop an alumina (92% pure, ε_r=9.5) hermetic package for a phase shifter chip (Figure 1). This package was reproduced using high resistivity silicon (ε_r=11.7). Figure 2

0-7803-4603-6/97/$5.00 (c) IEEE

shows the package layout (5 layers) and the through line used for characterization. A metal base is used for support, while an upper metallization layer and top lid are used to seal the package. A silicon substrate layer is used for RF input/output and DC bias lines. A hole is etched through the wafer for chip placement and a set of six micromachined vias are placed along the left and right of the IC for electromagnetic shielding. These vias are used in the seal frame layer as well. A center hole in the seal frame is etched for IC placement and two outer holes are used for wafer probing. The package dimensions are 7.112 x 7.112 x 1.27 mm. The alumina and silicon package differ in bias line width (smaller for silicon) and three ultrasonic wire bonds are used to connect the silicon package and IC as opposed to four in the alumina package. The vias and input/output microstrip feedline in the alumina package are displaced from the center for application reasons whereas the square vias and feedline are symmetric in the silicon design.

Conventional thin lm processing technology is utilized to fabricate the package. A 50 ohm through line is used to characterize the effect of the package which incorporates sections of microstrip, stripline and shielded microstrip. Silver epoxy is used to attach the lid and provide the connection between the upper and lower metallization surfaces (electromagnetic shielding). Given the measurement setup, a 50 ohm grounded coplanar waveguide (GCPW) to microstrip transition is used (Figure 3). Via holes are etched to provide connection between the upper and lower metal surfaces. The via holes required in this package are developed by anisotropic etching using ethylene diamine pyrocatechol (EDP). Three microns of electroplated Au are used as the metallization for the package and IC (through line) (Figure 4).

3.0 Results

The silicon package described earlier is characterized experimentally using an HP8510C Network Analyzer, and an Alessi probe station with 150 mm pitch GGB Picoprobes. A Thru-Re ect-Line (TRL) calibration was performed to deembed effects up to the open microstrip feedline.

Figures 5 and 6 show the insertion loss and return loss, respectively, for the alumina and silicon-based package. Over the whole frequency range, the insertion loss of the silicon package is better than that of the alumina package by 0.5 dB. The return loss for the silicon package is mostly attributed to the ohmic loss of the through line for which measured values are shown in Figure 7. The observed irregularity in the alumina package suggests parasitic effects not related to impedance mismatch. The estimated cost for the Si package (batch processing) is less than $1 and re ects a substantial reduction compared to conventional co red ceramic packages.

4.0 Conclusion

We have shown that it is possible to develop silicon-based packages for discrete components using thin lm processing and micromachining techniques. This effort is less expensive and outperforms its HTCC counterpart. This packaging approach can be extended to provide advanced packaging techniques where discrete as well as integrated components can be hosted by the same silicon wafer.

5.0 Acknowledgements

This work has been supported by contracts from the Army Research Of ce and the Of ce of Naval Research.

References

[1] J.G. Yook, L.P.B. Katehi, et. al., Experimental and Theoretical Study of Parasitic Leakage/Resonance in a K/Ka-Band MMIC Package, *IEEE Trans. on Microwave Theory and Techniques*, Vol. 44, No. 12, December 1996.

[2] M.I. Herman, K.A. Lee, et. al., Novel Techniques for Millimeter-Wave Packages, *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 7, July 1995.

[3] R.F. Drayton, L.P.B. Katehi, Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques, *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 9, September 1995.

[4] K.E. Petersen, Silicon as a Mechanical Material, *Proceedings of the IEEE*, Vol. 70, No. 5, May 1982.

[5] J.E. Licari, *Multichip Module Design, Fabrication and Testing*, Mc-Graw Hill, Inc., New York, 1995.

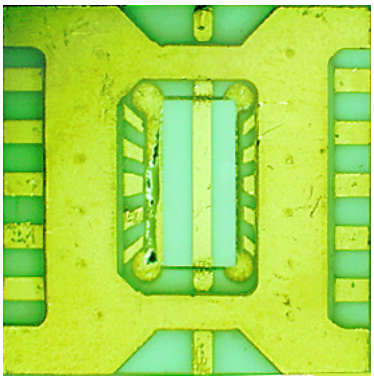

Figure 1 HTCC hermetic package designed by NASA Lewis.

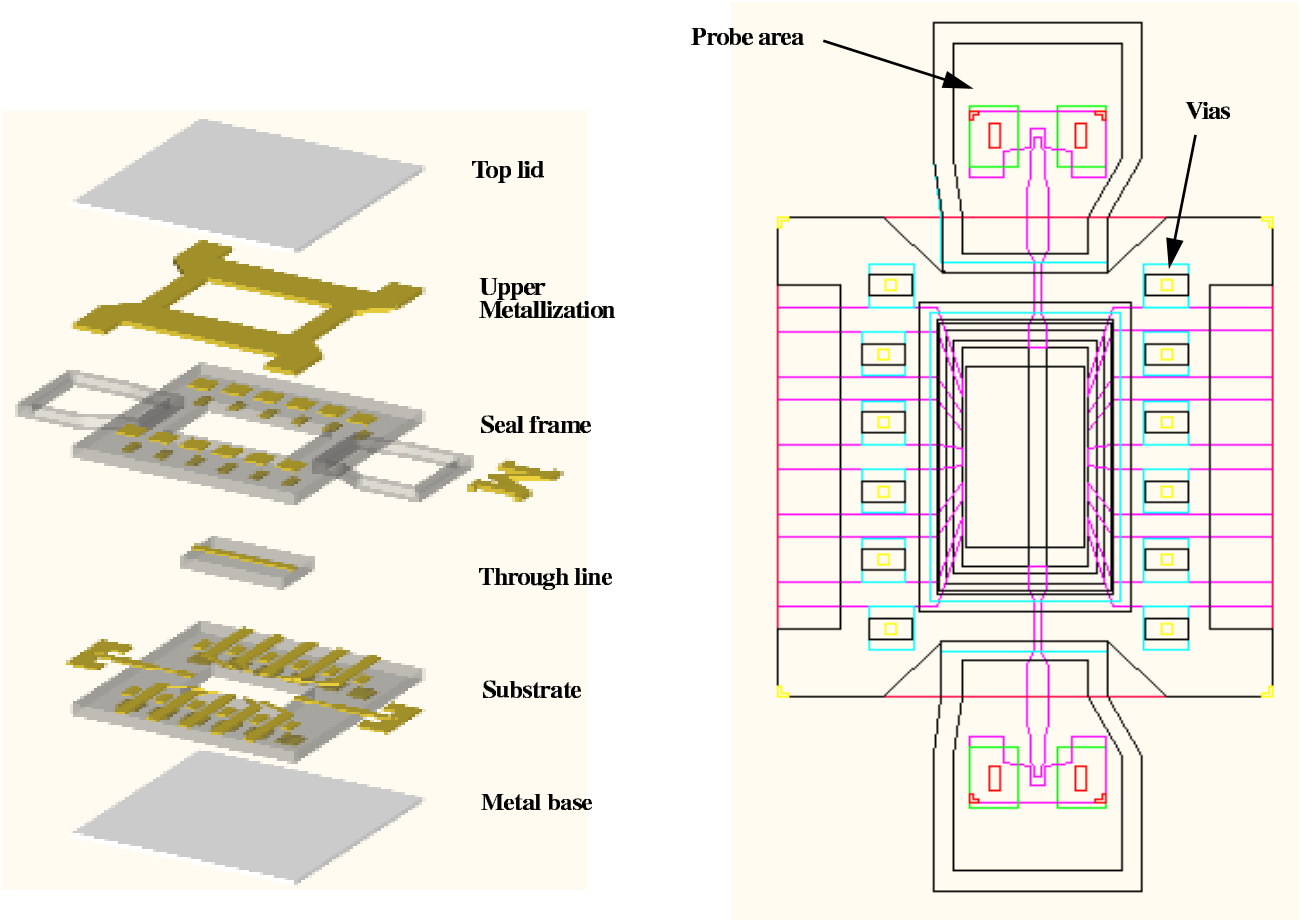

Figure 2 3-D view of package layers and actual CAD drawing with all layers superimposed.

Figure 3 Photograph of probe window with GCPW to microstrip transition for on-wafer probing.

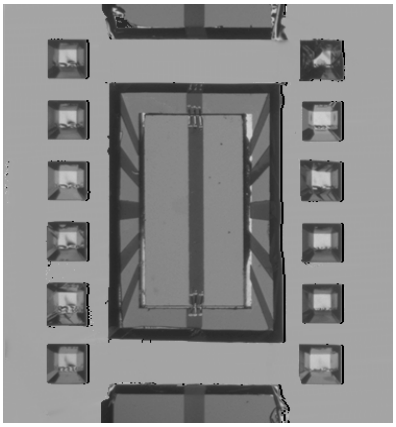

Figure 4 Micromachined silicon-based package.

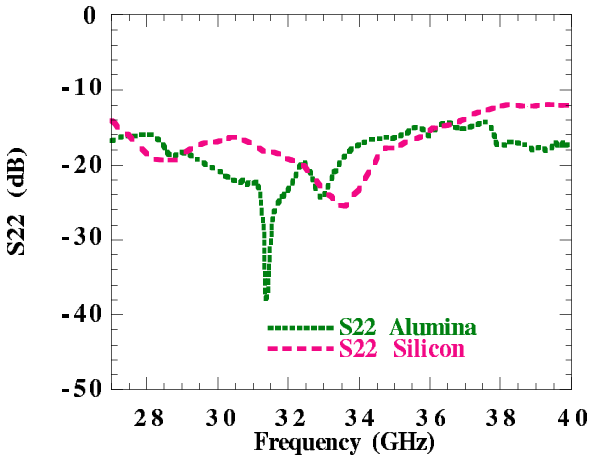

Figure 6 Return Loss

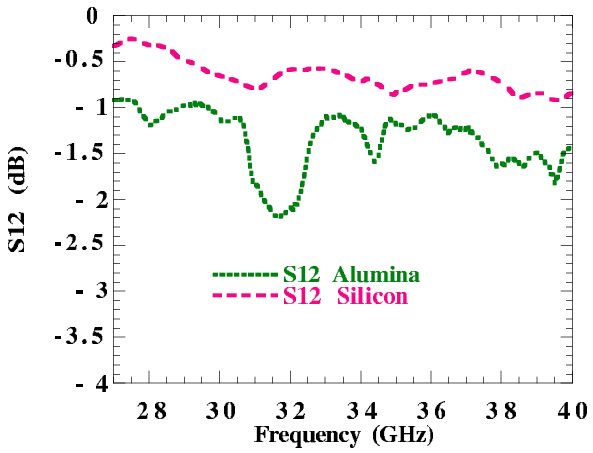

Figure 5 Insertion Loss

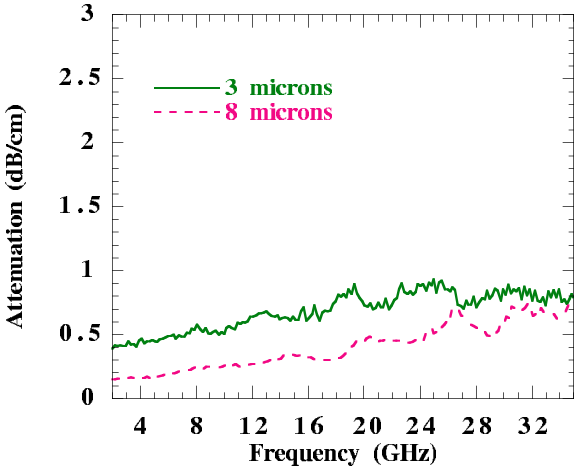

Figure 7 Attenuation of 9 mm through line in package.